# Lab 08 – Worksheet

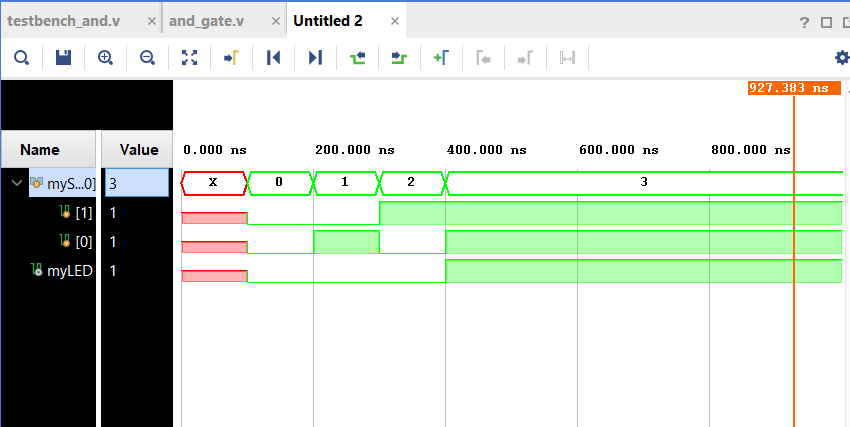
|  |  |  |
| --- | --- | --- |
| Name: Ali Muhammad Asad  Shayan Shoaib Patel | ID: aa07190  sp07101 | Section: T6 |

## Programming Basys-3 board

In this report, include following:

* Snapshot of simulation output of AND Gate.
* Add all codes related to adder subtractor
  + Design Modules
  + Constraint Files

**AND Gate Simulation Output**



**Adder\_Subtracter - Design File Code**

`timescale 1ns / 1ps

module addSubtract(

input [2:0] A,

input [2:0] B,

input O, // takes usual O for -/+ sign

output [6:0] myLED, // output for LED

output dP // for the output sign

);

wire [2:0] C; // inner carriers

wire [2:0] sum;

wire [2:0] D;

wire [3:0] X;

wire carry, E, Y ;

complement u1(O, B, C);

three\_bit\_adder u2(A ,C ,sum ,carry);

assign dP = ~O || carry;

assign E = ~O & carry;

assign X = {E ,D};

complement u3(~dP , sum, D);

seven\_segment u6(X , myLED);

endmodule

**Adder\_Subtracter – Constraint File Code**

set\_property IOSTANDARD LVCMOS33 [get\_ports {A[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {A[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {A[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {B[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {B[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {B[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports dP]

set\_property IOSTANDARD LVCMOS33 [get\_ports O]

set\_property IOSTANDARD LVCMOS33 [get\_ports {myLED[6]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {myLED[5]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {myLED[4]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {myLED[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {myLED[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {myLED[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {myLED[0]}]

set\_property PACKAGE\_PIN V17 [get\_ports O]

set\_property PACKAGE\_PIN V7 [get\_ports dP]

set\_property PACKAGE\_PIN R2 [get\_ports {A[2]}]

set\_property PACKAGE\_PIN T1 [get\_ports {A[1]}]

set\_property PACKAGE\_PIN U1 [get\_ports {A[0]}]

set\_property PACKAGE\_PIN W2 [get\_ports {B[2]}]

set\_property PACKAGE\_PIN R3 [get\_ports {B[1]}]

set\_property PACKAGE\_PIN T2 [get\_ports {B[0]}]

set\_property PACKAGE\_PIN W7 [get\_ports {myLED[0]}]

set\_property PACKAGE\_PIN W6 [get\_ports {myLED[1]}]

set\_property PACKAGE\_PIN U8 [get\_ports {myLED[2]}]

set\_property PACKAGE\_PIN V8 [get\_ports {myLED[3]}]

set\_property PACKAGE\_PIN U5 [get\_ports {myLED[4]}]

set\_property PACKAGE\_PIN V5 [get\_ports {myLED[5]}]

set\_property PACKAGE\_PIN U7 [get\_ports {myLED[6]}]

**Assessment Rubrics**

**Marks Distribution:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  |  | **LR2**  **Code/Simulation (In-Lab)** | **LR5**  **Results** | **LR7**  **Viva** | **LR9**  **Report** |
| **In-lab** | **Task b** | - | 10 points | 10 points | 10 points |
| **Task c** | - | 10 points |
| **Task d** | 20 points | 10 points | 30 points |
| **Total marks 100** |  | 20 | 50 | 10 | 40 |

**Marks Obtained:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  |  | **LR2**  **Code/Simulation (In-Lab)** | **LR5**  **Results** | **LR7**  **Viva** | **LR9**  **Report** |
| **In-lab** | **Task b** | - |  |  |  |
| **Task c** | - |  |
| **Task d** |  |  |  |
| **Total marks 100** |  |  |  |  |  |